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FAIRCHILD SEMICONDUCTOR™

October 1987
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CD4029BC
Presettable Binary/Decade Up/Down Counter

General Description

The CD4029BC is a presettable up/down counter which counts in either binary or decade mode depending on the voltage level applied at binary/decade input. When binary/decade is at logical "1", the counter counts in binary, otherwise it counts in decade. Similarly, the counter counts up when the up/down input is at logical "1" and vice versa.

A logical "1" preset enable signal allows information at the "jam" inputs to preset the counter to any state asynchronously with the clock. The counter is advanced one count at the positive-going edge of the clock if the carry in and preset enable inputs are at logical "0". Advancement is inhibited when either or both of these two inputs is at logical "1". The carry out signal is normally at logical "1" state and goes to logical "0" state when the counter reaches its maximum count in the "up" mode or the minimum count in the "down" mode provided the carry input is at logical "0" state.

All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Features

- Wide supply voltage range: 3V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility: fan out of 2 driving 74L or 1 driving 74LS
- Parallel jam inputs
- Binary or BCD decade up/down counting

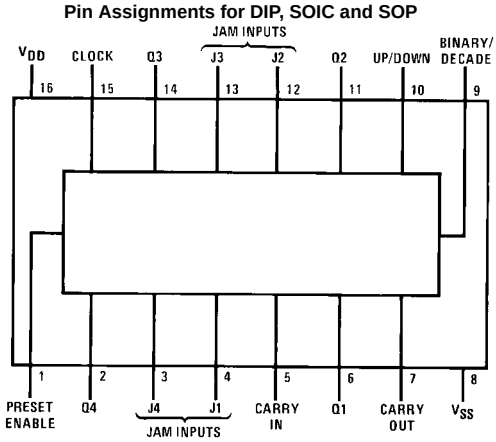
Ordering Code:

Order Number	Package Number	Package Description
CD4029BCWM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide body
CD4029BCSJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4029BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC and SOP



Top View

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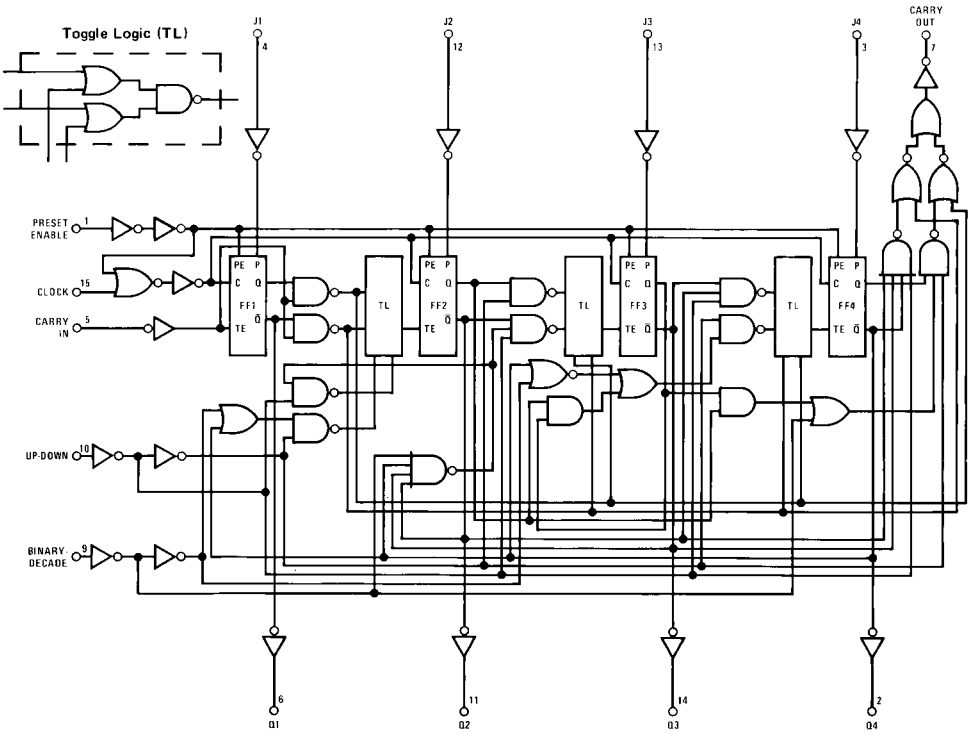
Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

DC Supply Voltage (V_{DD})	−0.5V to +18 V_{DC}
Input Voltage (V_{IN})	−0.5V to V_{DD} + 0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15 V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	−40°C to +85°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	µA
		V_{DD} = 10V		40			40		300	µA
		V_{DD} = 15V		80			80		600	µA
V_{OL}	LOW Level	$\|I_O\|$ < 1 µA								
	Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level	$\|I_O\|$ < 1 µA								
	Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	LOW Level	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
	Input Voltage	V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	HIGH Level	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
	Input Voltage	V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	LOW Level Output	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
	Current (Note 3)	V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level Output	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
	Current (Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	µA

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 4)

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$k, Input $t_{rCL} = t_{fCL} = 20$ ns, unless otherwise specified

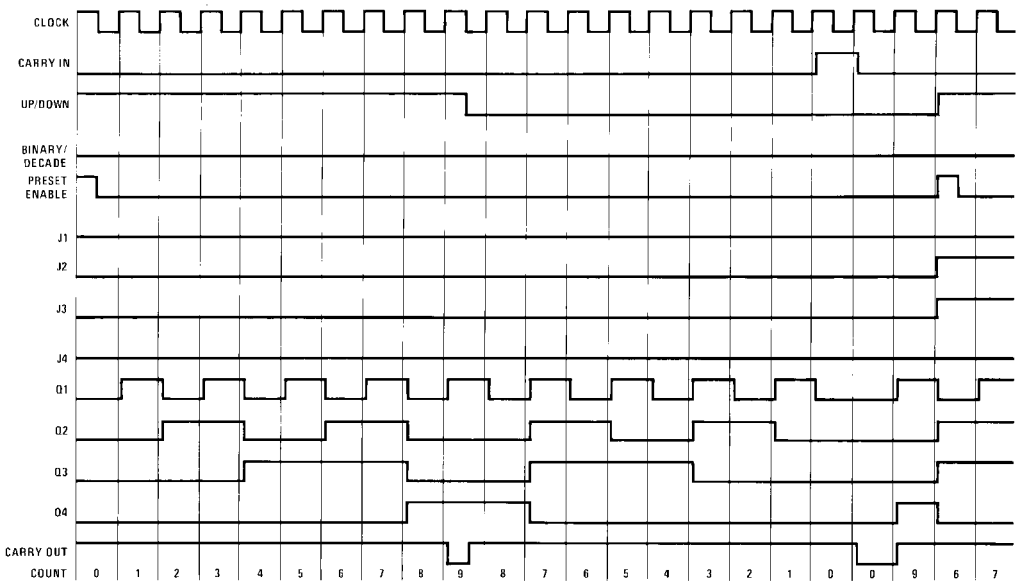
Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCKED OPERATION						
t_{PHL} or t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		200	400	ns
	to Q Outputs	$V_{DD} = 10V$		85	170	ns
		$V_{DD} = 15V$		70	140	ns
t_{PHL} or t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		320	640	ns
	to Carry Output	$V_{DD} = 10V$		135	270	ns
		$V_{DD} = 15V$		110	220	ns
t_{PHL} or t_{PLH}	Propagation Delay Time	$C_L = 15$ pF				
	to Carry Output	$V_{DD} = 5V$		285	570	ns
		$V_{DD} = 10V$		120	240	ns
		$V_{DD} = 15V$		95	190	ns
t_{THL} or t_{TLH}	Transition Time/Q	$V_{DD} = 5V$		100	200	ns
	or Carry Output	$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WH} or t_{WL}	Minimum Clock	$V_{DD} = 5V$		160	320	ns
	Pulse Width	$V_{DD} = 10V$		70	135	ns
		$V_{DD} = 15V$		55	110	ns
t_{rCL} or t_{fCL}	Maximum Clock Rise	$V_{DD} = 5V$	15			µs
	and Fall Time	$V_{DD} = 10V$	10			µs
		$V_{DD} = 15V$	5			µs
t_{SU}	Minimum Set-Up Time	$V_{DD} = 5V$		180	360	ns
		$V_{DD} = 10V$		70	140	ns
		$V_{DD} = 15V$		55	110	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1.5	3.1		MHz
		$V_{DD} = 10V$	3.7	7.4		MHz
		$V_{DD} = 15V$	4.5	9		MHz
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 5)		65		pF
PRESET ENABLE OPERATION						
t_{PHL} or t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		285	570	ns
	to Q output	$V_{DD} = 10V$		115	230	ns
		$V_{DD} = 15V$		95	195	ns
t_{PHL} or t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		400	800	ns
	to Carry Output	$V_{DD} = 10V$		165	330	ns
		$V_{DD} = 15V$		135	260	ns
t_{WH}	Minimum Preset Enable	$V_{DD} = 5V$		80	160	ns
	Pulse Width	$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	ns
t_{REM}	Minimum Preset Enable	$V_{DD} = 5V$		150	300	ns
	Removal Time	$V_{DD} = 10V$		60	120	ns
		$V_{DD} = 15V$		50	100	ns
CARRY INPUT OPERATION						
t_{PHL} or t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		265	530	ns
	to Carry Output	$V_{DD} = 10V$		110	220	ns
		$V_{DD} = 15V$		90	180	ns
t_{PHL}, t_{PLH}	Propagation Delay Time	$C_L = 15$ pF				
	to Carry Output	$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		85	170	ns
		$V_{DD} = 15V$		70	140	ns

Note 4: *AC Parameters are guaranteed by DC correlated testing.

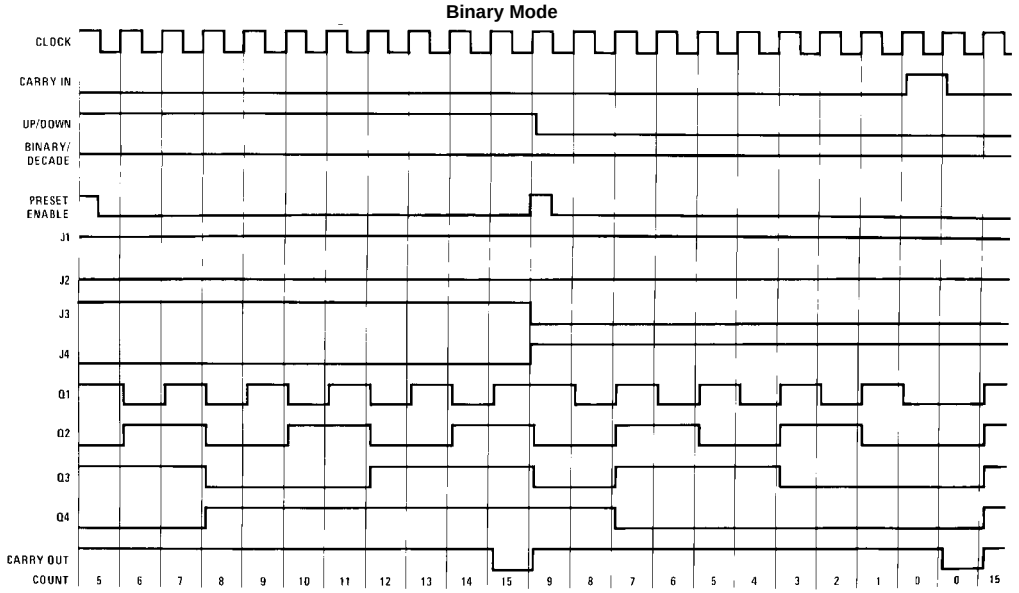
Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 74C Family Characteristics application note, AN-90.

Logic Waveforms

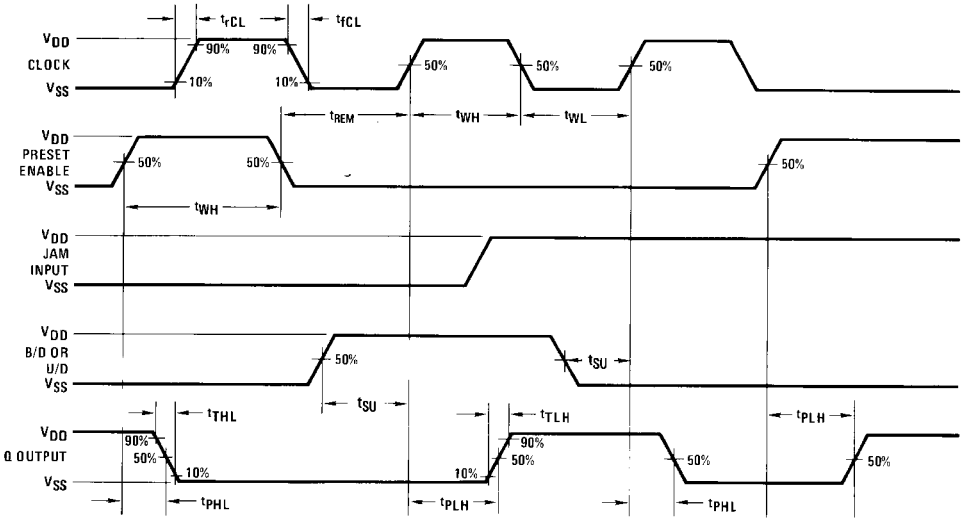
Decade Mode



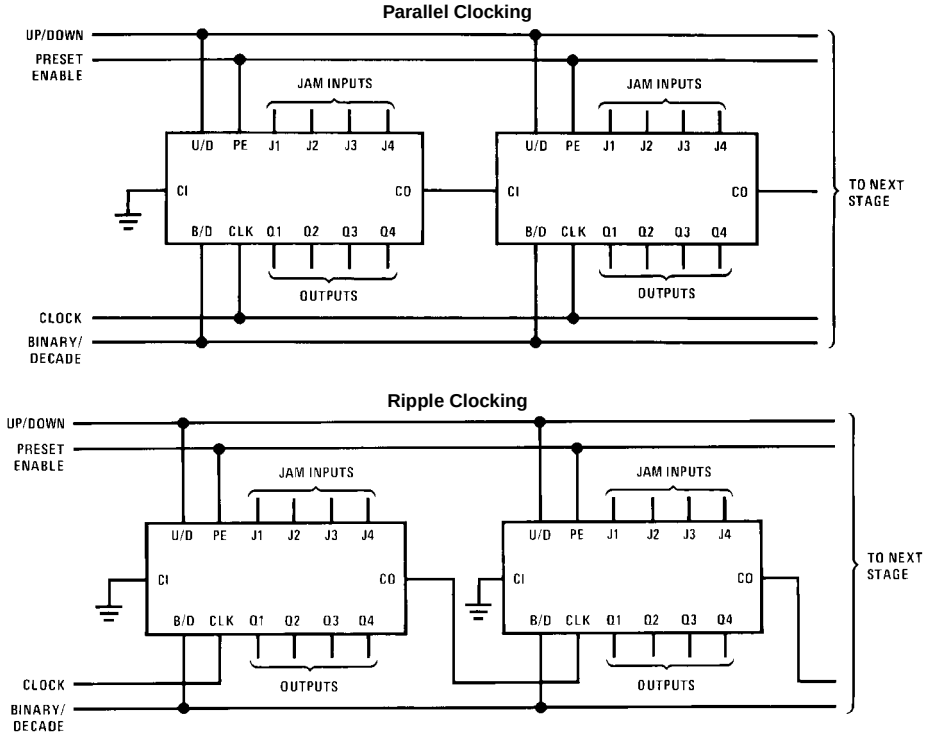
Binary Mode



Switching Time Waveforms

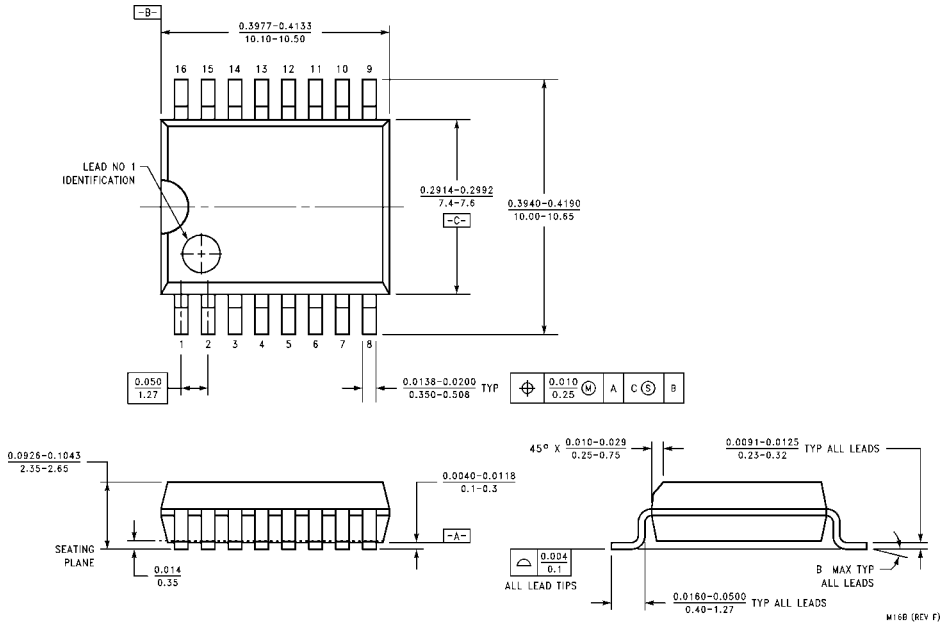


Cascading Packages

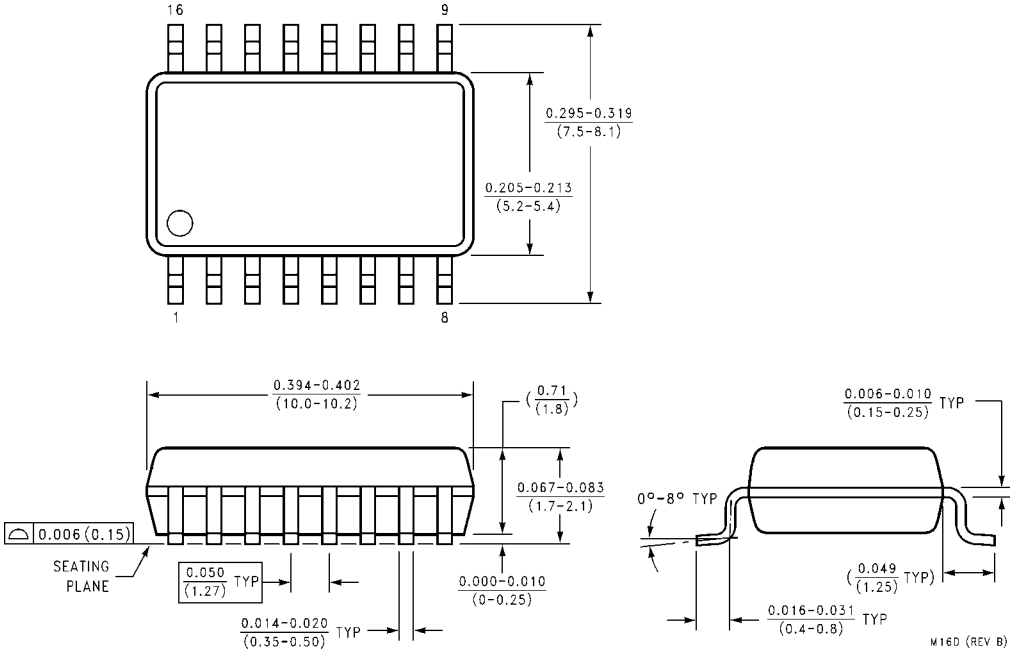


Carry out lines at the 2nd or later stages may have a negative-going spike due to differential internal delays. These spikes do not affect counter operation, but if the carry out is used to trigger external circuitry the carry out should be gated with the clock.

Physical Dimensions inches (millimeters) unless otherwise noted

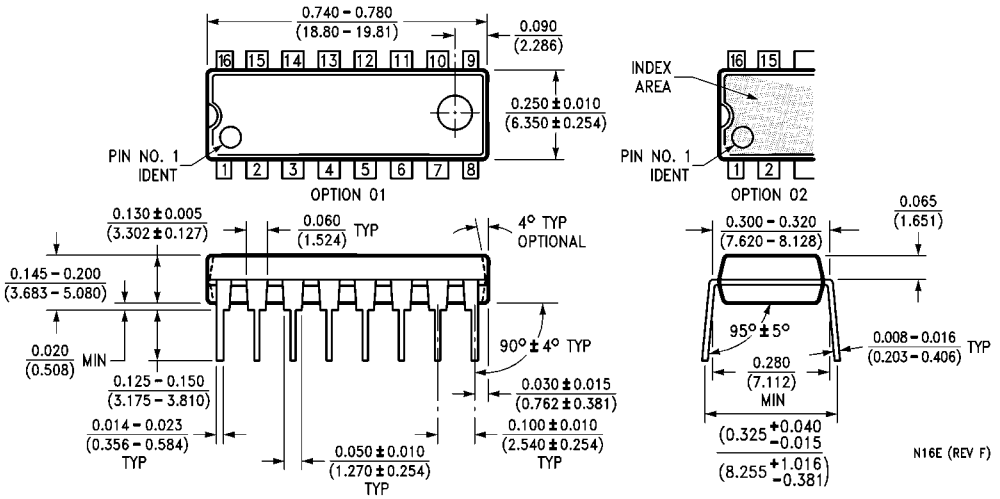


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M16B



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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